ABSTRACT OF THE DISCLOSURE

A multi-chip system and method are disclosed that utilizes a plurality of graphics pipelines to perform large kernel convolution. Each graphics pipeline includes a standard rendering unit and a video data convolve unit. Each video data convolve unit receives video pixel data from the video output of the standard rendering unit. The video data convolve units are connected in a chain. Each group of one or more video data convolve units in the chain convolves the video pixel data received by the group. The last video data convolve unit in the chain outputs a stream of convolved pixels.